Listing of Claims:

1. (Currently amended) A thin film semiconductor device, comprising:

a substrate;

a conductive type semiconductor layer provided on the substrate and having a ~~sectorial or~~ trapezoidal planar shape including a long side, a short side, and an opening angle of at least 20 degrees; and

a transistor with a source region and a drain region in ~~on~~ the ~~conductive type~~ trapezoidal semiconductor layer ~~provided~~ wherein either the source region is on the long side and drain region is on the short side or the source region is on the short side and the drain region is on the long side ~~such that electric current flows along a grain boundary~~.

2. (Currently amended) A thin film transistor, comprising:

a crystallized conductive type semiconductor layer having a trapezoidal planar shape with a long side, a short side, and an opening angle of at least 20 degrees;

a source region and a drain region provided in the trapezoidal semiconductor layer, wherein either the source region is on the long side and drain region is on the short side or the source region is on the short side and the drain region is on the long side;

~~a conductive type semiconductor layer;~~

~~a source region and a drain region that are separately provided in the semiconductor layer such that electric current flows along a grain boundary;~~

a gate electrode provided above or below the semiconductor layer with an insulating film interposed therebetween; and

wherein a channel region is located between the source region and the drain region and a first junction face extends between the source region and the channel region and has a first junction face width, and a second junction face extends between the channel region and the drain region and has a second junction face width, and wherein the first junction face width differs from the second junction face width.

3-4. (Canceled)

5. (Previously presented) A thin film transistor as claimed in claim 2, wherein the semiconductor layer includes one or more grain boundaries each of which extends in one of the following two directions: (1) from the source region to the drain region and (2) from the drain region to the source region of the semiconductor layer.

6. (Canceled)

7. (Previously presented) A thin film transistor as claimed in claim 2, wherein the semiconductor layer includes at least two grain boundaries, each of which extends in one

of the following two directions: (1) from the source region to the drain region and (2) from the drain region to the source region of the semiconductor layer, and wherein at least two of the grain boundaries are adjacent to each other and extend in-plane with the semiconductor layer in correspondence with an opening angle.

8. (Previously presented) A thin film transistor as claimed in claim 2, wherein the semiconductor layer includes at least two crystal grain boundaries, each of which extends in one of the following two directions: (1) from the source region to the drain region and (2) from the drain region to the source region of the semiconductor layer, the semiconductor layer further including two grain boundaries adjacent to each other and in parallel with an in-plane direction of the semiconductor layer.

9. (Currently amended) A thin film transistor as claimed in claim 5, further including a first angle formed by ~~(1) an~~ a first imaginary line connecting the middle of the first junction face width ~~and (2) an imaginary line connecting~~ with the middle of the second junction face width and a second imaginary line extending in the direction of the grain boundary, and a second angle being an opening angle defined by respective imaginary lines connecting first ends of the first junction face width and second ends of the second junction face width, wherein the difference between the two angles is at least 20 degrees.

10-18. (Canceled)

19. (Currently amended) A thin film transistor as claimed in claim 7, further including a first angle formed by ~~(1) an~~ a first imaginary line connecting the middle of the first junction face width ~~and (2) an imaginary line connecting~~ with the middle of the second junction face width and a second imaginary line extending in the direction of the grain boundary, and a second angle being an opening angle defined by respective imaginary lines connecting first ends of the first junction face width and second ends of the second junction face width, wherein the difference between the two angles is at least 20 degrees.

20. (Currently amended) A thin film transistor as claimed in claim 8, further including a first angle formed by ~~(1) an~~ a first imaginary line connecting the middle of the first junction face width ~~and (2) an imaginary line connecting~~ with the middle of the second junction face width and a second imaginary line extending in the direction of the grain boundary, and a second angle being an opening angle defined by respective imaginary lines connecting first ends of the first junction face width and second ends of

the second junction face width, wherein the difference between the two angles is at least 20 degrees.

21. (Previously presented) A thin film transistor as claimed in claim 2 forming part of a liquid crystal display.

22. (Previously presented) A thin film transistor as claimed in claim 5 forming part of a liquid crystal display.

23. (Previously presented) A thin film transistor as claimed in claim 9 forming part of a liquid crystal display.

24. (Previously presented) A thin film transistor as claimed in claim 2 forming an N-type transistor.

25. (Previously presented) A thin film transistor as claimed in claim 2 forming a P-type transistor.

26. (New) A thin film transistor as claimed in claim 19 forming part of a liquid crystal display.

27. (New) A thin film transistor as claimed in claim 20 forming part of a liquid crystal display.

28. (New) A thin film transistor as claimed in claim 2 wherein the gate electrode is configured to cover an entire surface of the channel region.

29. (New) A thin film transistor as claimed in claim 5 wherein the gate electrode is configured to cover an entire surface of the channel region.

30. (New) A thin film transistor as claimed in claim 7 wherein the gate electrode is configured to cover an entire surface of the channel region.

31. (New) A thin film transistor as claimed in claim 2 wherein the semiconductor layer is formed from an amorphous semiconductor film crystallized by a laser beam exhibiting a weaker intensity at its center than at its periphery.

32. (New) A thin film transistor as claimed in claim 5 wherein the semiconductor layer is formed from an amorphous semiconductor film crystallized by a laser beam exhibiting a weaker intensity at its center than at its periphery.